International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 3, No. 3, September 2013, pp. 328 – 335
ISSN: 2088-8694

Soft Switched Multi-Output PWM DC-DC Converter

Rashmi Sharma

Electrical and Electronics Engineering, Indus University, Ahmedabad, India

Article Info

Article history:

Received Jul 20, 2013
Revised Aug 17, 2013
Accepted Aug 28, 2013

Keyword:

Pulse Width Modulation (PWM)
Push-Pull converter
Magnetic Amplifier

ABSTRACT

In this paper, a new soft switched cell that overcomes most of the drawbacks of the normal "hard switched-pulse width modulation" converter is proposed to contrive a new family of soft switched PWM converters. All of the semiconductor devices in this converter are turned on and off under exact or near zero voltage switching (ZVS) and/or zero current switching (ZCS). No additional voltage and current stresses on the main switch and main diode occur. A push-pull converter equipped with the proposed snubber cell is analyzed in detail. The predicted operation principles and theoretical analysis of the presented converter are verified with a prototype of a 50W PWM push-pull multi-output converter with insulated MOSFET and for regulation of slave outputs magnetic amplifier post regulators are considered as post regulators. Moreover; this multioutput converter has a simple structure, low cost, and ease of control circuitry.

Corresponding Author:
Rashmi Sharma
Electrical and Electronics Engineering
Indus University, Ahmedabad, Gujarat, India
Email: rashmi.electnirma@gmail.com

1. INTRODUCTION

Pulse width modulated (PWM) DC-DC converters have been increasingly used as switched-mode power supplies in industry. The PWM technique is identified for its high power capability, ease of control circuitry, higher power density and faster transient response, this can be achieved by increasing the switching frequency. However, as the switching frequency increases, so do the switching losses and EMI noise. High switching losses reduce the power capabilities, while serious EMI noise interferes with the control of PWM DC/DC converters.

To solve the problems resulting from the non ideal phenomena of switching losses, several kinds of soft-switching technologies have been adapted which are shown in different papers [3]. Out of these technologies active clamps, as introduced in [4] can reduce all three loss mechanisms by using auxiliary switches. Unfortunately, an auxiliary switch increases the complexity of both power and control circuits as well as synchronization problems between control signals of the two switches during transient also complicate the control strategy. The circuit cost is increased and the reliability is decreased by using these active snubber techniques. Although many technologies came one by one to reduce these losses as one of the cheapest technique is by using resistors, capacitors, and diodes (RCD) as a snubber but could not perform well despite of having the simplest structures as the switching losses are dissipated in resistors and thus, it reduces the efficiency of the circuit. Other techniques comprised of resonant converters that commutate with either zero voltage switching (ZVS) or zero current switching (ZCS) are also introduced to reduce the switching losses; however conduction losses are increased in these circuits due to the high circulating current involved in it. Also complicated design of an EMI filter and control circuit because of a wide switching frequency range can cause great trouble in assessment of the circuit. Therefore compared with the three

technologies discussed above, the introduced novel soft switching technique can effectively restrict switching losses and EMI noise using no active components and no power dissipative components [5]. By increasing the rates of the drain current and the drain source voltage restricted by inductors and capacitors, respectively.

The control strategy is scarcely interfered with and the circulating energy generated is comparatively low. The circuit structure is as simple as RCD snubber and the efficiency is as high as zero voltage and zero current soft switched and resonant converters. Low cost, high performance and high reliability are the distinct advantages of this novel soft switching technique to reduce the turn off losses caused in push pull converter.

The problem of the regulation of multiple output voltages is solved here with the help of mag-amp post regulator. Mag-amp circuits with square wound core is become popular in medium to high power application where the limited efficiency of the linear regulators is not acceptable. The Mag Amp regulation principle offers a low cost, efficient and, owing to the simple design, reliable solution to these problems. The low RF interference level is advantageous to the suppression filter; a mag amp comes the closest yet to a true ideal switch with significant benefits to switching regulators [8].

2. DESIGN SPECIFICATIONS

The following design review focuses on the design procedure of a three-output DC/DC converter for different applications. The desired specifications include input bus of 70V±2V, output in the range of +5.0V/3.5A, -5.0V/2.5A, +10V/1.5A. Total output power is 45W and line regulations better than ±0.5%and load regulation better than ±1.0% is considered for design with ripple noise better than 20mV and overall efficiency >75% The block diagram of the PWM based multi-output DC-DC Converter is as shown in Fig. 1:

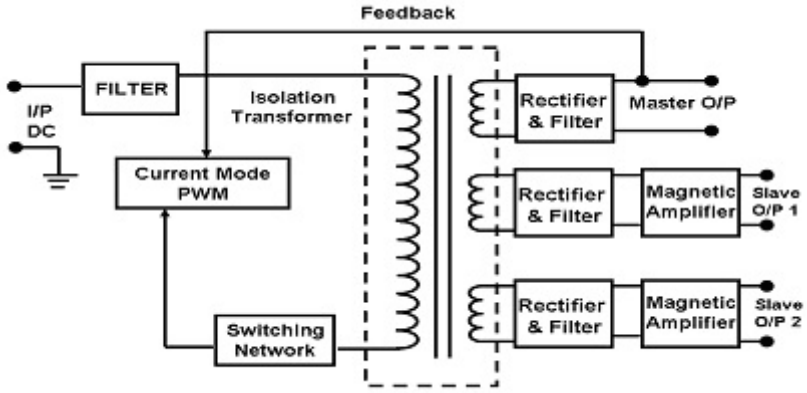

Figure 1. Block Diagram of PWM based DC-DC Converter

3. WORKING OF THE SOFT SWITCHED CIRCUIT

Soft switching circuit to reduce the turn off losses of the push pull converter, as shown in Fig. 1, provide a appropriate solution to this problem. Just as does the other soft switched converters do with the active switches without making the circuit more complex with the isolated driver circuitry, it also provides the advantages of soft switching circuit, as they use a capacitor to slow up collector voltage rise time. It changes the stored electrostatic energy on the capacitor into electromagnetic energy in the form of stored current in an inductor. Then later in time (but before the next cycle when the capacitor must again be discharged), the inductor current is forced to discharge its stored current back into the DC input bus. Thus no energy is wasted-it is first stored on a slow-up capacitor, and then returned back with negligible loss to the input bus. The details of soft switching circuit connections are shown in Fig. 2.

The following initial conditions are assumed for simple analysis as; MOSFET Q1 is the ideal switch and there is no leakage or stray inductance in transformer. The Q1 is now at on condition and Vcr is a negative voltage Vcn. The drain voltage Vdc is equal to Vdc because ic = 0 and ip = 0 since there is no current owing into Cr, Lr, and the primary side of transformer T1, .Here the operation is shown in Fig. 3 for only one cycle of the switch. The operating modes can be divided into four time slots as shown in the following sections.

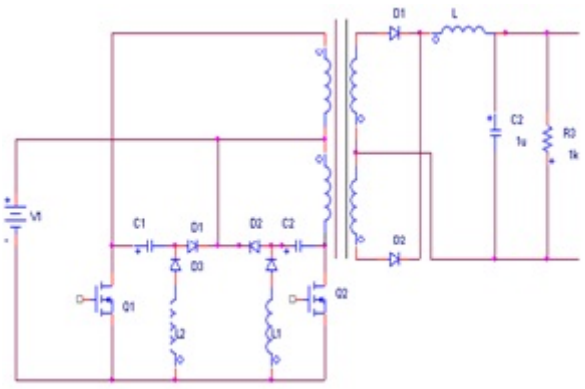

Figure 2. Soft switching circuit for push pull converter

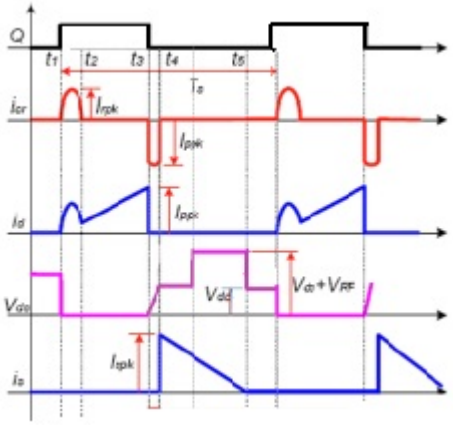

Figure 3. Operation of single cycle of switch

3.1. MODE 1 (t1 ≤ t < t2):

If Q_1 is turned on at t = t_1, the C_r is resonated from -V_{RF} with L_r through D_2 and Q_1. The resonant time and the peak current I_{rpk} can be calculated as;

$$T_1 = T_2 - T_1 = /pi\sqrt{L_r \times C_r} = \frac{1}{2f_r} \tag{1}$$

$$I_{rpk} = \frac{V_{rf}}{Z_r} = (V_o + V_d) \times \sqrt{(\frac{C_r}{L_r})(\frac{L_p}{L_s})} \tag{2}$$

where f_r and Z_r are a resonant frequency and a resonant impedance, respectively, VD is the voltage drop in Do and V_{RF} is the reflected voltage from secondary winding to primary winding . In circuit, the primary side current, ip, starts from zero. A resonant current also starts from zero. Also the total mosfet drain current starts also starting from zero with a resonant fashion. The drain voltage, V_{ds}, becomes immediately zero when $Q_1$is turned on. However, there is almost no voltage and current crossing area when Q_1 is switched off because of the slow starting current. If the resonant current is reached at a peak level, the C_r voltage become zero and is charged with a positive value up to the reflected voltage V_{RF}.

3.2. MODE 2 (t2 ≤ t <t3):

If i_{cr} becomes zero, the C_r voltage is charged to V_{cp}. The primary side current is increased with the slope of the ratio of V_{ds} to L_p. Hence the peak current I_{ppk} of the primary side can be calculated as

$$Ippk = \frac{V_{dc}}{L_p} \times T_{on} \tag{3}$$

$V_a = V_{c1} = V_{RF}$ where L_p is a primary inductance of transformer T_1 and T_{on} is the turn-on time of mosfet Q_1. The Mode 2 duration, $T_2 = T_3 - T_2$, depends on the control duty cycle. The Va voltage is equal to V_{c1} because the negative port of C_1 is connected to ground through Q_1. When $Q_1$is turned off, this mode is finished.

3.3. MODE 3 (t3 ≤ t <t4):

As soon as Q_1 is turned off, the current flowing into the primary side becomes a constant current source charging C_r through D_1 . This current amplitude is the same as the peak current I_{ppk}. The voltage, V_{C1}, is linearly changed from a positive V_{RF} to a negative V_{RF} .In a conventional push pull converter, a major switching loss occurs when Q_1 is turned off since the highest drain current is crossed with the highest drain voltage. Furthermore, the mosfet Q_1 is turned on under the maximum drain current level.

However, the drain voltage, V_{ds}, is slowly increased with a slope because of charging time of C1 in the lossless passive snubber circuit. This provided slope creates a low turning off switching loss. Therefore, the efficiency can be improved by providing this time, $T_3 = T_4 - T_3$, with the lossless snubber circuit. In this mode, the output voltage, Va, becomes V_{dc} because diode D_1 is turned on. The drain voltage V_{ds} is increased up to $V_{dc} + V_{RF}$. If the forward voltage drop, V_D, across the diode, D_o, is assumed as 0.5, then the peak voltage V_{dpk} of V_{ds} can be calculated as

$$V_{dpk} = V_{ds} + V_{RF} = V_{dc} + (Vo + 1)\sqrt{\frac{L_p}{L_s}} \tag{4}$$

where L_p and L_s are the inductances of the primary and secondary side transformer, respectively. If the drain to source capacitor is assumed small compared with C_r, the Mode 3 duration time, T_3, can be found as following:

$$T_3 = T_4 - T_3 = 2V_{RF} \times \frac{C_r}{I_{ppk}} \tag{5}$$

This mode is finished when V_{c1} = -V_{RF} or $V_{ds} = V_{dpk}$.

3.4. MODE 4 (t4 ≤ t <t5):

The secondary side output circuit is now conducting with the starting current level of I_{spk} as soon as V_{dc} is equal to V_{dc}+ V_{RF}. This current can be calculated from I_{ppk} by using the ratio of primary to secondary inductances as follows:

$$I_{spk} = I_{ppk} \times \frac{Np}{Ns} = I_{ppk}\sqrt{\frac{L_p}{L_s}} \tag{6}$$

The load current is now decreased from I_{spk} to zero as follows:

$$is(t) = I_{spk} - \frac{V_o}{L_s} \times (t - t4) \tag{7}$$

Va = V_{dc}-V_{RF}

The load current becomes zero at T_4 . If the average load current, I_o, and primary peak current, I_{ppk}, are known by using (3), then this mode duration time, T_4, can be calculated by using an integration of $I_{spk}$for one switching time, T_s, as

$$T_4 = T_5 - T_4 = 2T_s\frac{I_o}{I_{spk}} \tag{8}$$

4. WORKING PRINCIPLE OF MAGNETIC AMPLIFIER

Regulating multiple outputs of a switching power supply has always presented an additional challenge to the designer. With a single pulse-width modulated control system, how can the control loop be configured to keep all outputs in regulation when each may have varying loads? Although it is sometimes possible to average an error signal from each output -degrading the regulation on some outputs to improve on others a

more common approach, is to close the overall power supply loop to the output with the highest load current and opt for some form of auxiliary -or secondary - regulation for all the other outputs.

Post regulation techniques are based on closed loop output voltage regulation of their respective outputs and are briefly discussed in paper [5]. A popular and effective application of the Square-Perm alloy 80 tape wound cores occurs in multiple-output switched-mode power supplies. By using such a square loop core to provide a controllable delay at the leading edge of the pulses at the secondary of the transformer, one or more outputs can be independently and precisely regulated the output power, without the losses inherent in linear regulators or the complexity of conventional switching regulators. In cases where the load currents of the subordinate outputs are high (in excess of one or two amps), the advantages of the saturable-core regulators become more and more significant [7] and [8].

4.1. Mag Amp Design

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time have reduced the costs of what might have been ruled out as too expensive in the past. Some considerations affecting the choice of core material are subjected in paper [8].

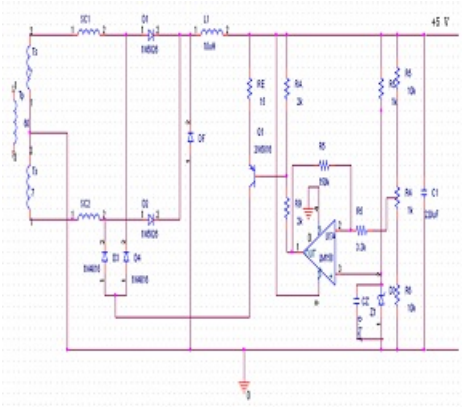

Figure 4. Secondary end of transformer circuit having magnetic amplifier

Push pull saturable core regulator for slave output1 -5V is shown in Fig. 4 which is driven by two magnetic amplifier cores, error amplifier and NPN transistor. In the pulse width modulated (PWM), the primary pulse width is controlled by sensing the 5V output,comparing it to a reference and using the error signal to adjust the pulse duration. If there is no saturable core (SC) in the circuit the slave output 5V would be semi regulated since the primary control loop provide line regulation. But the output would vary with load and temperature. To provide -5V Vdc at the output the average value of the rectified waveform applied to the input inductor L must be -5V. The pulse height at the secondary of transformeris given by

$$V_s = (V_{in}) \times (\frac{N_s}{N_p}) \tag{9}$$

$$PW = (\frac{5V \times 10us}{2 \times 8.4V}) = 2.9\mu s \tag{10}$$

Because the input pulse is of 4us wide the SC must delay the leading edge by 1μs. Since the amplitude of the pulse is 8.4V, we can say the core must withstand 8.4V*1μs=8.4Vμs. To accomplish this core is reset by an amount during each cycle. As the input of the core swings negative, diode clamps the output side of the core at +6.3V. As Vr = 8.4Vμs/4μs =2.1V, Vr = -Vc + Vs = +6.3V The reset of the core is subjected to a reverse voltage of 2.1V for a duration of 2.1V*4μs=8.4Vμs. As the input varies, the error amplifier will alter this value to ensure that the output is regulated at -5Vdc in spite of changes in rectifier voltage drop.If, for any reason, the DC output voltage goes up, firing time must go down, which means that blocking Time must go up. Thus, if the DC output voltage goes up, the error-amplifier output goes down and the Q2 collector current goes up, pushing more reset current into the no-dot end of MA. This pushes the initial flux level B, down further, increases blocking time, thus decreasing firing time and bringing the DC output voltage back down. Similarly, of course, a decrease in Vos, causes an increase in

error amplifier output voltage and a decrease in Q2 reset current. As B, flux level rises, tb decreases, firing time increases, and Vos, is brought back up. All this, of course, occurs over a number of switching cycles and is accomplished in a time dependent on the error- amplifier bandwidth. Similarly Slave output-2 is regulated against load change.

5. MEASUREMENT RESULTS

The line regulation of the multi output push pull regulator is within the limit specified in the objective and for load regulation Magnetic amplifier is incorporated as post regulator for slave outputs for better load regulation. Here magnetic amplifier circuit is tested for different load conditions and results are compared with the linear regulators. At input voltages ranges from 68V to 72V are measured under full load condition and results are compared with convectional push pull converter Comparision of secondary output voltage with and without post regulation is shown in Fig. 5 where channel 1 shows waveform at transformer end and at the end of the saturable core. Table I shows the load and line regulation of multi-output converter.

Table 1. Load and Line regulation of multi-output converter

Specifications	Line regulation ≤0.5%	Load regulation ≤1.0%
Master output	0.2	0.5
Slave-1 output	0.4	0.4
Slave-2 output	0.3	0.7

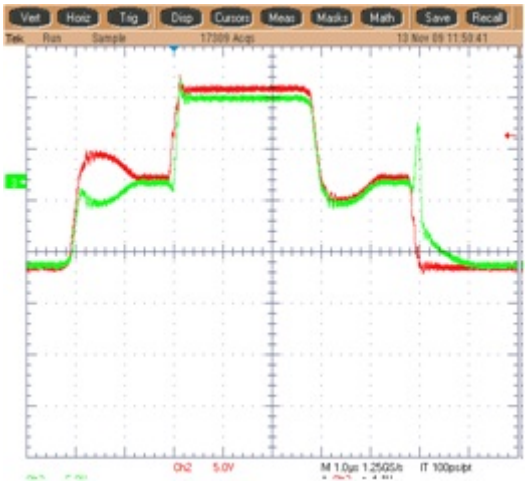

Figure 5. Secondary output voltage waveform,Channel 1 shows waveform at transformer end and channel 1 at the end of the saturable core

A switching loss may occur when MOSFET is turned off under the peak resonant drain voltage condition. In a worst case, this resonant drain voltage can be very high, up to almost Vdc+VRF. However this drain voltage resonance with high frequency is effectively alleviated by using an additional parallel path of Lr and Cr to the primary side inductance with the drain-to-source capacitor. The drain voltage can be kept at the Vdc level just before Q1 is turned off. By observing the Fig. 5 it is shown that the turn on time of the MOSFET is increased by introducing lossless circuit comprised of inductor, capacitor and diodes. The waveforms in Fig. 6 show the turn ON time of the switch with 100ns but with the lossless circuit the ON time is increased unto 336ns. Here, the drain to source voltage is increased with a slope because of charging time of the capacitors in the lossless passive snubber circuit.This provide slope creates a low turn on switching losses. Here, the maximum efficiency calculated is 82%, where as efficiency obtained with convectional technique is 79%.

The experimental results show that the voltage peak level as well as a swing frequency caused by a leakage inductance and stray capacitance can be reduced. The graph plotted in between with and without soft switching network in Fig. 7 shows this efficiency improvement. Hence, the results obtained by soft switching network shows that the efficiency is slightly improved by 3%.

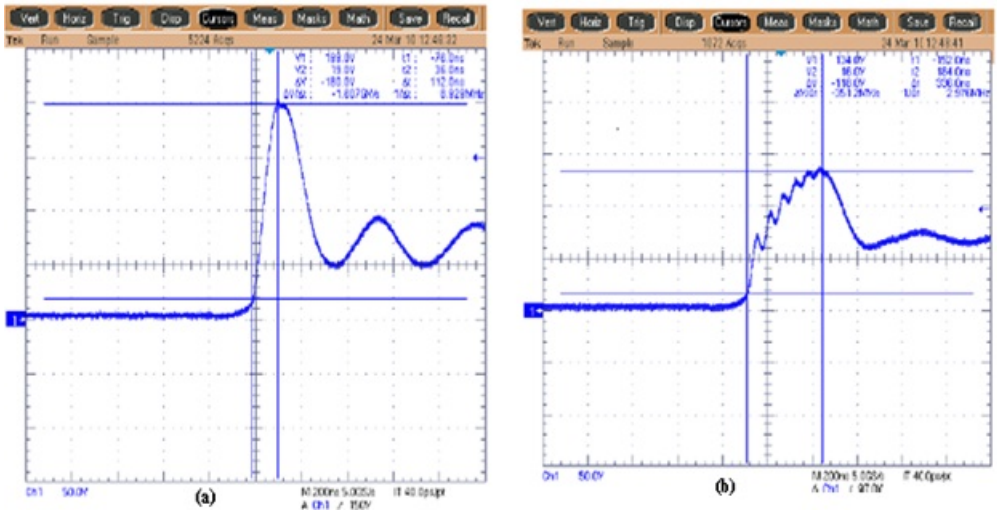

Figure 6. Waveform: Drain to Source terminal of the MOSFET

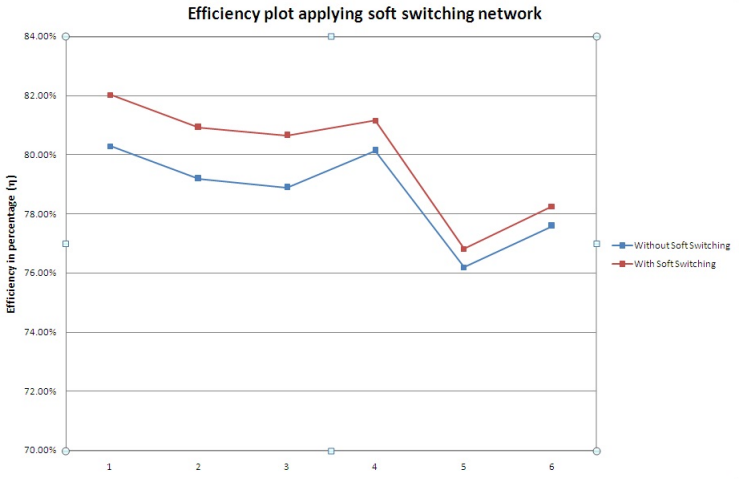

Figure 7. Efficiency plot with and without soft switched converter

6. CONCLUSION

This topic has presented the most frequently used topologies for multi-output power supply design. This snubber circuit can not only reduce the turn-on and turn-off losses of power devices, but can also remove snubber losses in the converter. This snubber circuit allows the design of very simple, low-cost, high efficiency switch-mode power supply. Additionally, at full output power this soft switching converter has overall efficiency, which is about 75% in the hard switching case, increases to about 81%. The completed prototype circuit and the measurement results proved the effectiveness of the presented approached the benefits of the selected topology.

REFERENCES

[1] Pressman A., Switching Power Supply Design, *McGraw Hill*, 2nd Ed, 2007
[2] Chryssis George, High-Frequency Switching Power Supplies, *McGraw Hill*, Ed 1987
[3] Lenk Ron, Practical design of power supply, *McGraw Hill*, 2nd Ed, IEEE press, 1998
[4] Balogh Laszlo ,Design Review: 140 W, Multiple Output High Density DC/DC Converter, *Texas Instruments Incorporated*, 2001
[5] In Hwan Oh, Loss less snubber circuit in flyback converter and its utilization for low operating voltage, *Fair child semiconductor*, 1997
[6] Zho X.and Xu P., A Novel Current-sharing Control Technique for Low-voltage High-current Voltage

Regulator Module Applications, *IEEE Trans. On Power Electronics*, Vol. 15, Nov-2000
[7] Peterson William A.and Plaskon Steven L.,"Dual Charge Mode Control of A Current Fed Boost-Buck Push Pull Converter, *IEEE Trans. On Power Electronics*, pp. 1595 1603,Jan-1998,
[8] Tedder R. M., Limitations of the Magamp Regulator and an Improved Magamp Choke Design Procedure, *Powertechnics*, November and December, 1988.
[9] Jamerson C., Calculation of Magnetic Amplifie, Post Regulator Voltage Control Loop Parameters, *Proceedings of the Second International High Frequency Conference*, pp. 222-234, Washington, D.C., April, 1987.

BIOGRAPHY OF AUTHOR

Rashmi Sharma received her B.E. Degree in Electrical Engineering from Oriental Institute of Technolgy, RGPV, Bhopal and subsequently completed her M.Tech. in Electrical Engineering from Nirma University, Ahmedabad in year 2010. She has successfully completed her M.Tech. industrial training in the field of power electronics for space usages in Space Applications Centre, Indian Space Research Organisation (ISRO), Ahmedabad. She joined Indus University as an Assistant Professor in Electrical and Electronics Engineering Department in year 2010.